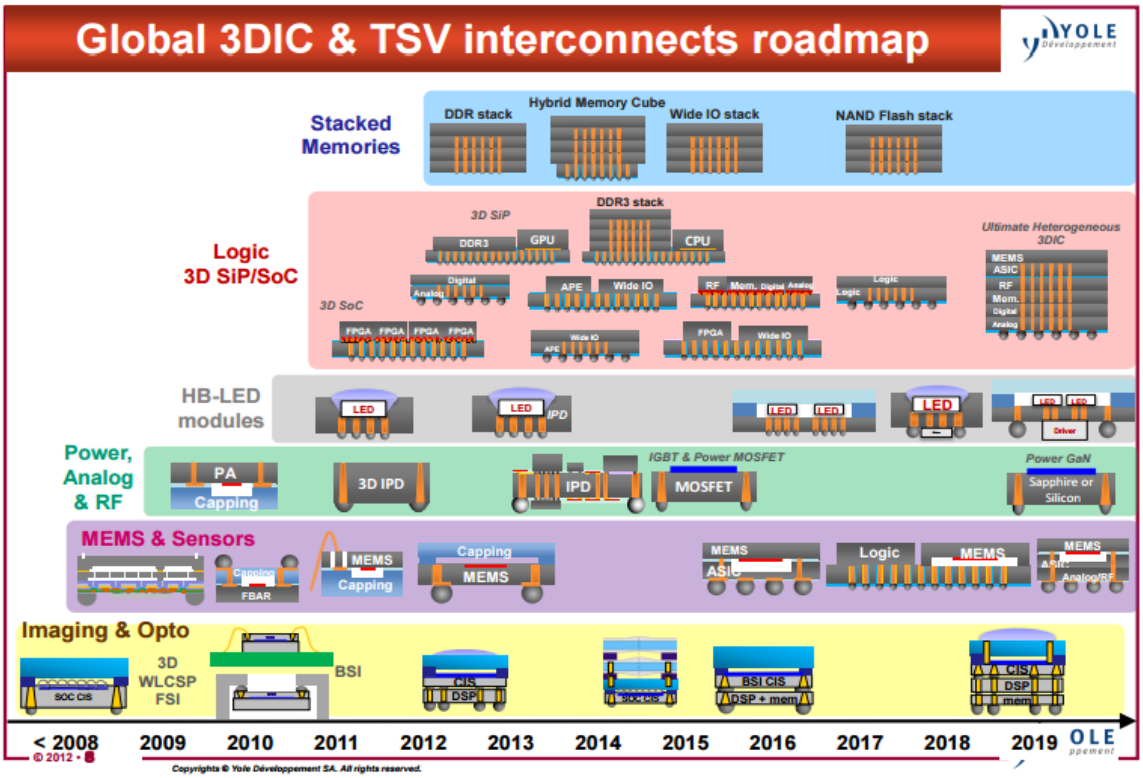
# 3D IC Packaging




SOURCE : YOLE

Through Silicon Vias (TSV) technology was adopted in production a few years ago for MEMS and CMOS Image Sensors (CIS). Driven by consumer applications such as smartphones and tablets, this market have grown over the last several years. 3DIC adoption & implementation has been seen for high-end memories (HBM/HBC) from 2014. Standards have now been established, the industry has grown in high-volume manufacturing. Wide I/Os, logic-on-logic will follow, and Heterogeneous 3DIC nowadays is heating up. EPTC 2016 has lined up short courses on 3DIC integration / 3DIC Packaging & FA methods for 2.5D/3DIC and invited papers / speakers to present on the TSV / 3DIC integration on Advanced technology node. Full details are in the subsequent pages.

# PROFESSIONAL DEVELOPMENT COURSES

Professional Development Course 2

30nd November 2016 – 08:30 to 12:20hrs.

## 3D Integrated Circuits Failure Analysis

Ingrid De Wolf, Prof

imec, Belgium & KULeuven, Belgium

**Course description:**

In 3D stacked-IC technology, thinned Si wafers/dies are vertically interconnected offering faster and more compact electronic circuits with heterogeneous integration capabilities. The stacked wafers/dies are electrically interconnected using µ-bumps and Cu TSVs (Through Silicon Vias). However, the introduction of these new materials and new fabrication schemes is associated with new failure mechanisms requiring new failure analysis (FA) techniques. In addition, even for well-known failures in 2D-chips, pin-pointing the failure location becomes increasingly challenging because of a combination of inaccessibility of the devices (part of a 2.5D or 3D stack) with small dimensions and high density of the devices.

In this course, after a short introduction to 3D technology and failure analysis, various failure analysis techniques that can be used for FA of 3D technology are discussed in detail. Their principle is explained, the advantages and limitations for 3D technology-FA are discussed, and typical case studies are presented. The course will cover well known classical techniques, such as for example X-ray, scanning acoustic microscopy (SAM) and magnetic field imaging, but also new developments of these techniques. In addition, less conventional techniques (ex. lock-in thermography, polariscopy, EOTPR and some recent new electrical test-based techniques) will be covered.

## Course Outline:

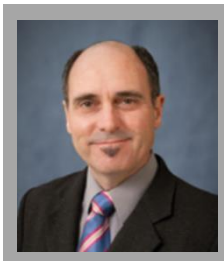
- Introduction
- 3D technology
  - short introduction to the technology (aim, TSV, micro-bumps, thinning and stacking, Cu pillars,...)
  - overview of expected failure mechanisms in 3D technology
- Failure analysis
  - what, why, 2D versus 3D
  - failure analysis sequence
  - challenges

- Overview of 3D FA techniques (+ case studies)
  - Infra-red microscopy
  - X-ray based techniques
  - Acoustic techniques (SAM, GHz SAM, acoustic signals)
  - Magnetic field/current imaging methods
  - TDR and EOTPR
  - Polariscopy
  - Photon emission microscopy
  - Lock-in thermography
  - New e-test based techniques
- Conclusions

**Biography:** Ingrid De Wolf received the PhD in Physics from the KU Leuven university, Belgium, in 1989. In the same year she joined imec in Belgium, where she worked in the field of microelectronics reliability, with special attention for gate oxide reliability, mechanical stress analysis using micro-Raman spectroscopy and failure analysis using emission microscopy. From 1999 to 2014, she headed the group REMO, where research is focused on reliability, test and modelling of 3D technology, interconnect, MEMS and packaging. She managed to grow this group from a small team of 3 members to a highly recognized group of about 40 people which is involved in several programs within imec (3D, interconnect, Optical IO, GaN, Litho, PV, MEMS, STT-MRAM...). She authored or co-authored 14 book chapters and more than 350 publications of which ~30 invited, and won several best paper awards at conferences focusing on reliability and failure analysis (ESSDERC, ESREF, ISTFA, EOS/ESD symposium, IEDM). She was often involved as session chair or technical committee member of these conferences, and is member of the steering committee of ESREF. She is chief scientist at imec, IEEE senior member and professor at the department of Metallurgy and Materials Engineering of the KU Leuven where she teaches courses on non-destructive testing, MEMS reliability and failure analysis, characterization techniques and FMEA.

Professional Development Course 6

30nd November 2016 – 13:10 to 17:00hrs.



# 2.5D- and 3D-Stacked Integrated Circuits

Paul Franzon

NCSU

**Abstract**

Three dimensional chips stacked using Through Silicon Via (TSV) technology has been under consideration and the subject of intensive research for several years now. This tutorial covers the technology, applications, design and CAD for 3DIC. The technology will be introduced, including TSVs, face to face technologies, integration options and interposers. Applications will be discussed as driven by cost, performance and power efficiency needs. Examples will be given from the commercial world and the author's own research. CAD and CAD-driven design will be covered including verification, test, and thermal evaluation.

Outline

1. 3DIC Motivation
    a) Power Efficiency
    b) Memory Bandwidth
    c) Bandwidth density
    d) Heterogeneous Integration
    e) Cost reduction
2. 3DIC Manufacturing
    a) Bulk TSV formation
    b) SOI TSV formation
    c) Wafer and chip assembly flows
    d) Interposers
3. 3DIC Design and Test
    a) Power and power efficiency
    b) Memories and memory interfaces
    c) The potential for logic partitioning
    d) CAD flows
    e) Thermal design
    f) Power delivery
4. Test
    a) Test issues
    b) Potential Test Flows
    c) Test standards
    d) Cost issues
5. Conclusions and Future perspectives

**Biography:** Paul D. Franzon is currently a Distinguished Professor of Electrical and Computer Engineering at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Adelaide, Australia. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom and three companies he cofounded, Communica, LightSpin Technologies and PBI Inc. His current interests center on the technology and design of complex microsystems incorporating VLSI, MEMS, advanced packaging and nano-electronics. He has lead several major efforts and published over 200 papers in these areas. In 1993 he received an NSF Young Investigators Award, in 2001 was selected to join the NCSU Academy of Outstanding Teachers, in 2003, selected as a Distinguished Alumni Professor, and received the Alcoa Research Award in 2005. He served with the Australian Army Reserve for 13 years as an Infantry Solider and Officer. He is a Fellow of the IEEE.

# KEYNOTE

## Advances of 3D Integration in CHINA

**Wenhui Zhu**

**Central South University, China**

With Moore's law coming to end, 3D integration becomes an approach to extend package performance. This keynote will report most recent progress in 3D integration packaging in China, mainly on multi-scaling thermal and reliability design, new process technologies for high aspect ratio micro-via manufacturing, and extreme wafer thinning. Formation of organic insulation layer in TSV(through silicon via) based on self-assembly chemical reaction will be discussed, simulation results of controllable via-filling through additives-energy-interaction will be presented. Selective-removing of Si-Cu-composed heterogeneous wafer by using nano-particles for back-grinding will be proposed and analyzed. A short review will also be given to TSV-CIS(CMOS Image Sensor) and Fingerprint sensors, the most important application areas of TSV technology.

**Biography:Dr. Wenhui Zhu**

Dr. Wenhui Zhu is the CEO of Speed Suzhou Semiconductor Technology Pte Ltd. and professor of Central South University, China. He is the Chief Scientist of "Fundamental Research on Wafer-Level 3D Integration for 20/14nm ICs" which is the 1st National Basic Research Program(973) in 3D IC integration. He was elected as Specially invited "1000 Elite Plan Expert(2011)" under top class Talent plan of China. Previously he was Chief Technology Officer of Tian Shui Hua Tian Technology Co. Ltd, CEO of Kun Shan Q Technology Limited Co. He has been working in TSV packaging, DFR (design for reliability), DFM (design for manufacturability) and DFP (design for performance), packaging materials and 3D nano-/micro-electronics packaging in leading semiconductor and packaging companies including Infineon, UTAC and TSHT. Dr. Zhu chaired many key projects in advanced packaging and structural integration such as national 863 project, Chinese natural science fund, and state key technology projects and made great achievements in technology innovation and cost-saving. He is a key player of international conferences, e.g. IEEE ICEPT(2008-now) and EPTC(2006-2009), as organization committee or technical committee chairman / co-chairman. Dr. Zhu is also reviewer of a few international journals in packaging areas. He has been invited to give keynote talks and short courses in international forums and conferences. Dr. Zhu has published more than 120 technical papers, owns 46 patents and won 3 times of best paper awards.

# INVITED PAPERS

## Enabling Design for Reliability in Advanced Interconnects for 3D IC and Next Generation Solar PV (Photovoltaics) Systems

Dr. Arief Suriadi Budiman

Singapore University of Technology and Design

**Technical Session:** 2nd December 2016, 13:40hrs

**Venue :** MR331

The importance of mechanics and reliability in the design of advanced engineering systems and devices goes beyond their functionality. When materials under operational conditions fail, which occur for any advanced systems (electronics, photonics, photovoltaics, mechanical or even biological), failures are almost always controlled by the mechanics of the materials – more and more true in advanced or nanoscale materials. Device/system makers have more and more thus realized that until they ship robust and reliable nanoscale systems/devices, they will not realize the true commercial values of their products. Thus the term was coined in the design community – Design for Reliability. To enable design for reliability for advanced systems/devices like 3D IC systems and next generation photovoltaics (PV) modules, it is important that we not only become great nanoresearchers and scientists, but also great nanodesigners – able to offer complete and elegant engineering solutions from ideas to beautifully working, robust and reliable nanodevices. One key to enable the successful implementation of advanced interconnects in 3D IC using the Through-Silicon Via (TSV) as well as in next generation PV systems is the control of the mechanical stresses. They could lead directly to integration issues as well as reliability concerns during the system's lifetime. More importantly, they could also impact the device/system's electrical performance through strain-induced electron mobility change in the silicon (in the case of TSV) and the photovoltaics performance through cell cracks in the silicon solar cells (in the case of solar PV). In an effort to shed light on these topics, stress characterization and mapping of the samples using ex situ and in situ synchrotron X-ray microdiffraction technique (in situ – ie. during operational and/or accelerated loading conditions of the device) are proposed. The synchrotron-sourced X-ray microdiffraction technique has been recognized to allow some important advantages compared to other techniques, namely stress measurement of individual Cu TSV as well as the silicon substrate surrounding it simultaneously at the submicron resolution, stress measurement in situ during annealing and while Cu TSV is still buried under the silicon substrate (mimicking the conditions of real device). In the case of silicon solar PV, this technique has been also recently recognized to allow important measurement to be done directly on the silicon solar cells while they are already encapsulated in the

laminate or module packages. Using this approach, we aim to gain fundamental understanding of the role of stresses and mechanics, and how they evolve through processes and integration as well as during operation/service of the device leading to the eventual catastrophic events of failure. This elementary understanding of the failure mechanisms would allow the robust construction of mechanistic-based accelerated models. Some examples involving other advanced interconnects in Back-End-Of-the-Line (BEOL) integration schemes as well as in next generation thin silicon solar PV technology will also be discussed highlighting how we could enable design for reliability using the synchrotron X-ray microdiffraction technique in advanced microelectronics and next generation thin solar PV systems.

**Biography**

Arief Suriadi Budiman received his B.S. in mechanical engineering from Institute of Technology, Bandung (ITB), Indonesia, his M.EngSc in materials engineering from Monash Univ., Australia and his Ph.D. in Materials Science and Engineering from Stanford University, CA in 2008. During his doctoral candidacy at Stanford's Department of Materials Science & Engineering under the supervision of Professor William D. Nix (MRS Von Hippel Award 2007), Dr. Budiman received several research awards (MRS Graduate Silver Award 2006, MRS Best Paper 2006) and contributed to several high-impact journal publications (Acta Materialia, Applied Physics Letters, Journal of Electronic Materials). He gave two symposium invited talks as well in the MRS spring and fall meetings in 2006. More recently Dr. Budiman has been awarded the prestigious Los Alamos National Laboratory (LANL) Director's Research Fellowship to conduct top strategic research for the energy and national security missions of the Los Alamos National Laboratory's. At the Center for Integrated Nanotechnologies (CINT) at Los Alamos, Dr. Budiman's research program involves nanomaterials for extreme environments with potential applications in advanced energy systems including for next generation nuclear power reactors. Currently, at Singapore University of Technology & Design (SUTD), Prof. Budiman is leading a dynamic, young group researching nanomaterials and nanomechanics and their implications for extending the extreme limits of materials as well as their applications in the next generation energy technologies (solar PV, extreme environments, energy storage, etc.). His work has also recently received the famed Berkeley Lab Scientific Highlights twice in May 2010 and June 2013 (the latter was for his novel, innovative characterization technique that enables thin silicon solar PV technology). His deep expertise in the synchrotron X-ray microdiffraction technique was also recently utilized to enable the first ever in situ measurements of mechanical stresses in the 3-D through-silicon via (TSV) Cu interconnect schemes in the world – the findings were reported in a publication in Microelectronics Reliability (2012) and now one of the most highly cited references in the field of TSV/3D Interconnect stress measurements. He has been invited to give invited lectures/seminars on 3D/TSV Interconnect in various international conferences (including IEEE IITC 2012, AVS Thin Films Users Group 2012, TMS Symposium for Emerging Interconnects and Packaging Technologies 2011 and SEMATECH Workshop on 3D Interconnect Metrology at SEMICON 2011). Dr. Budiman has authored/co-authored several high-impact journal publications (Acta Materialia, Solar Energy Materials & Solar Cells, Materials Science Engineering A), and contributed a book chapter on "Electromigration in Thin Films and Electronic Devices: Materials and Reliability," Woodhead Publishing, Cambridge, 2011. He has also recently published a book "Probing Crystal Plasticity at the Nanoscales – Synchrotron X-ray Microdiffraction" (Springer 2015). He has two U. S. Patents and one pending.

# INVITED PRESENTATION

## What's happening in TSV based 3D/2.5D IC packaging: Latest market & technology trends

Santosh Kumar

Yole Développement

**Technical Session:** 2nd December 2016, 13:40hrs

**Venue :** MR332

Through-silicon vias (TSVs) have now become the preferred interconnect choice for high-end memory. They are also an enabling technology for heterogeneous integration of logic circuits with CMOS image sensors (CIS), MEMS, sensors, and radio frequency (RF) filters. In the near future they will also enable photonics and LED function integration. The market for 3D TSV and 2.5D interconnect is expected to reach more than two million wafers in 2020, expanding at >20% CAGR. The growth is driven by increased by increased adoption of 3D memory devices in high-end graphics, high-performance computing, networking and data centers, and penetration into new areas, including fingerprint and ambient light sensors, RF filters, photonics and LEDs.

The presentation will explain the market's dynamics and give an overview of all segments and key markets of the TSV based 3D/2.5D IC packaging.

**Biography**

Santosh Kumar,
Senior Technology and Market Analyst, Yole Développement

Santosh Kumar is currently working as Senior Technology & Market Research Analyst at Yole Développement. He is involved in the market, technology and strategic analysis of the microelectronic assembly and packaging technologies. His main interest areas are advanced IC packaging technology including equipment & materials. He is the author of several reports on fan-out / fan-in WLP, flip chip, and 3D/2.5D packaging.

# INVITED PRESENTATION

## Wafer Bonding as an Enabler for Microsystems Packaging and Integration

Chuan Seng Tan

Nanyang Technological University

**Technical Session:** 2nd December 2016, 13:40hrs

**Venue :** 336

Wafer bonding has come a long way in semiconductor manufacturing. Broadly, it can be classified as direct or indirect bonding. With the emergence of 3D packaging, MEMS packaging, engineered substrate and monolithic integration, wafer bonding has increasingly played a pivotal role. In the first half of this talk, solderless copper bonding is discussed with emphasis on surface passivation with self-assembled monolayer and surface activation with inert plasma. Recent work on copper nano-particles and micro-particles mixture for die attach application is also discussed. A demonstration of TSV-less CMOS-MEMS stacking with metal bonding is showcased. In the second half of this talk, discussion on molecular bonding of silicon and non-silicon materials is discussed. Applications in engineered substrate and monolithic integration using molecular bonding are also presented.

**Biography**:

Chuan Seng Tan received his B.Eng. degree in electrical engineering from University of Malaya, Malaysia, in 1999. Subsequently, he completed his M.Eng. degree in advanced materials from the National University of Singapore under the Singapore-MIT Alliance (SMA) program in 2001. He then joined the Institute of Microelectronics, Singapore, as a research engineer where he worked on process integration of strained-Si/relaxed-SiGe heterostructure devices. In the fall of 2001, he began his doctoral work at the Massachusetts Institute of Technology, Cambridge, USA, and was awarded a Ph.D. degree in electrical engineering in 2006. He was the recipient of the Applied Materials Graduate Fellowship for 2003-2005. In 2003, he spent his summer interning at Intel Corporation, Oregon. He joined NTU in 2006 as a Lee Kuan Yew Postdoctoral Fellow and since July 2008, he was a holder of the inaugural Nanyang Assistant Professorship. In February 2014, he was promoted to the rank of Associate Professor (with tenure). His research interests are semiconductor process technology and device physics. Currently he is working on process technology of three-dimensional integrated circuits (3-D ICs) as well as engineered substrate for electronics-photonics integration. He authored and edited four books. He is an associate editor for Elsevier Microelectronics Journal (MEJ). He is a member of IEEE.