Panel Talk Highlights and China Semicon

(EETIMES.com)

In 2015, China imported nearly 70% of the world's chips with about $230 billion dollars, which is more than the spend on crude oil. To change this situation, several plans, e.g. "Made in China 2025" (MIC 2025), were published by China's State Council recently, to invest more than $100 billion in the semiconductor industry to reach its goal of playing a larger role in the global market. With the MIC 2025 plan, China is aiming to improve the self-sufficiency rate for ICs in the nation to 40% in 2020, and boost the rate further to 70% in 2025.

How these policies and investment will impact the current semiconductor industry? What's the Opportunities & Challenges for the packaging community? EPTC has set up a panel session to explore the answers: "Rise of China Semiconductor". There are also invited presentations to demonstrate current state-of-art of advanced packaging development in China.

Topics: Semicon statistics and projections in China, Government policies, Supply chain, Semiconductor manufacturing and Packaging technologies, Opportunities & Challenges for China and for other countries/areas.

Panel session chair: **Dr Zhu Wenhui, , CEO, Suzhou Speed Semiconductor Technology Co. Ltd, China**

Panel members:

1. **Tan Yong Tsong, Executive Director of IME (Singapore)**
2. **Santosh Kumar, Senior Analysis of Yole Development (France)**
3. **Bob Chylak, Vice President of KnS (US)**
4. **Kai Fai Ng, President of SEMI SEA (Singapore)**
5. **Albert Lan, Senior. Director of SPIL (Taiwan)**
6. **Lung Chu, President of SEMI CHINA (China)**

KEYNOTE

Advances of 3D Integration in CHINA

Wenhui Zhu

Central South University, China

With Moore's law coming to end, 3D integration becomes an approach to extend package performance. This keynote will report most recent progress in 3D integration packaging in China, mainly on multi-scaling thermal and reliability design, new process technologies for high aspect ratio micro-via manufacturing, and extreme wafer thinning. Formation of organic insulation layer in TSV(through silicon via) based on self-assembly chemical reaction will be discussed, simulation results of controllable via-filling through additives-energy-interaction will be presented. Selective-removing of Si-Cu-composed heterogeneous wafer by using nano-particles for back-grinding will be proposed and analyzed. A short review will also be given to TSV-CIS(CMOS Image Sensor) and Fingerprint sensors, the most important application areas of TSV technology.

Biography:Dr. Wenhui Zhu

Dr. Wenhui Zhu is the CEO of Speed Suzhou Semiconductor Technology Pte Ltd. and professor of Central South University, China. He is the Chief Scientist of "Fundamental Research on Wafer-Level 3D Integration for 20/14nm ICs" which is the 1st National Basic Research Program(973) in 3D IC integration. He was elected as Specially invited "1000 Elite Plan Expert(2011)" under top class Talent plan of China. Previously he was Chief Technology Officer of Tian Shui Hua Tian Technology Co. Ltd, CEO of Kun Shan Q Technology Limited Co. He has been working in TSV packaging, DFR (design for reliability), DFM (design for manufacturability) and DFP (design for performance), packaging materials and 3D nano-/micro-electronics packaging in leading semiconductor and packaging companies including Infineon, UTAC and TSHT. Dr. Zhu chaired many key projects in advanced packaging and structural integration such as national 863 project, Chinese natural science fund, and state key technology projects and made great achievements in technology innovation and cost-saving. He is a key player of international conferences, e.g. IEEE ICEPT(2008-now) and EPTC(2006-2009), as organization committee or technical committee chairman / co-chairman. Dr. Zhu is also reviewer of a few international journals in packaging areas. He has been invited to give keynote talks and short courses in international forums and conferences. Dr. Zhu has published more than 120 technical papers, owns 46 patents and won 3 times of best paper awards.

INVITED PAPER

Packaging and Testing of High Speed Rotor for MEMS Gas Turbine Engines

Yan Xiaojun

Beihang University, China

Technical Session: 2nd December 2016, 8:30am

Venue : MR334

Abstract

MEMS gas turbine with its diameter of 1 cm, was firstly proposed by MIT, and will be one of the most promising propulsion or power system for Micro Air Vehicle and other Lab-on-Chip systems because of its higher power density. A micro rotor with high rotation speed is of vital importance for MEMS gas turbine engine to achieve its higher power density and transfer energy with high efficiency. In this investigation, a micro silicon rotor, which is fabricated by one-time multi-depth silicon etching method and supported by a 3-wafers bearing system, is completed to reach high rotation speed. To ensure wafer bonding quality, a non-destructive method based on analyzing infrared images through multilayer wafers is proposed and practiced. After the rotor and its bearing system are packaged successfully, a platform which consists of the rotor, the 3-wafers bearing system, air supply and control systems is established for testing and optimizing performance of the high speed micro rotor. The platform's control scheme is closed-loop and is based on the principle of stiffness changing, in which the stiffness of the bearing system is varied by adjusting inlet pressure based on the rotation speed.

Biography: Xiaojun Yan

Prof. Xiaojun Yan joined Beihang University in 2002 and is now a professor at the School of Energy and Power Engineering and vice-dean of the school. He received his B.S. and Ph.D. degrees from Beihang University in 1995 and 2000, respectively. He was a visiting scholar at UC Berkeley during 2009-2010. He was awarded the National Excellent 100 Doctoral Dissertation (2003) and the New Century Excellent Talents in Universities (2006) in China, the Second Prize for Progress in Science and Technology awarded by Chinese Ministry of Education (2013). He won the Beijing Youth May 4th Medal (2009), the Award for Beijing Talents in Education Innovation (2006). His current research interests include power and propulsion for micro air vehicles, smart structure, high temperature structure mechanics etc. Currently, he serves as a subject editor for Journal of Aerospace Power, and a member of Beihang University Academic Committee.

INVITED PRESENTATION

Advanced MIS SIP Technology

YB Lin

JCET, China

Technical Session: 1st December 2016, 13:40pm

Venue : MR331

Abstract

Molded Interconnect System (MIS) packaging is advanced semiconductor packaging technology and mature in semiconductor industry from 2011 and its superior electrical and thermal performance accommodates radio frequency (RF) and power management application. With innovative era coming, the demand for next generation semiconductor devices is driving lower cost, higher performance and increased functions including input/output (I/O) density, higher bandwidths and low power consumption as well as challenging packaging technology to create MIS Panel Packaging without packaging border for achieving the product marketing demand. Advanced Molded Interconnect System (MIS) SIP Packaging Technology is an innovative solution using Cu metal and molded compound MIS panel with full steel carrier on backside for robust transportation in packaging processes that enables ultra-thin SIP packaging and 3D SIP packaging. Furthermore, the advanced MIS SIP packaging will be introduced and compare current advanced packaging technologies to understand how and when to adopt this technology for achieving value semiconductor packaging.

Biography: YB Lin

YB Lin, senior director of packaging technology from JCET, possesses over 60 IP and 20 years' work experience of semiconductor packaging.