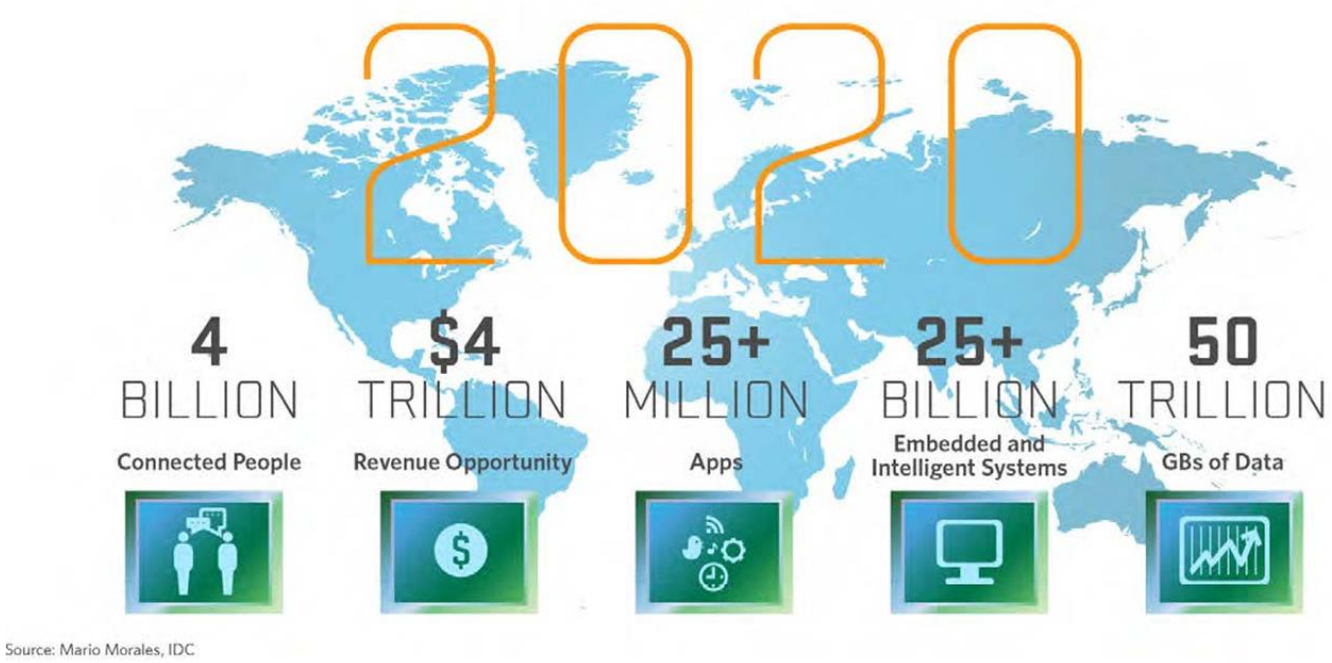
Internet of Things

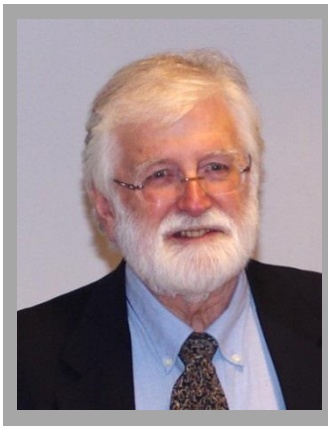


The Internet of Things (IoT) is the network of physical objects or "things" embedded with electronics, software, sensors, and network connectivity, which enables these objects to collect and exchange data. The size and cost of electronic components that are needed to support capabilities such as sensing, tracking and control mechanisms, play a critical role in the widespread adoption of IOT for various industry applications. EPTC 2016 has lined up a keynote speaker, 2 PDC courses, and series of invited papers & presentations to present on the internet of things from packaging perspective. Full details are in the subsequent pages.

PROFESSIONAL DEVELOPMENT COURSES

Professional Development Course 1

30nd November 2016 – 08:30 to 12:20hrs.



Nanotechnologies for Microelectronics Packaging Applications: Current trends in IoT, Wearable, 3D, Flex Circuits, Thermal and Embedded passives

James E. Morris

Portland State University, USA

Course Description: The course begins with an introduction to electronics packaging for context, which includes the current trends in IoT, wearable, 3D, flex circuits, thermal and embedded passives. It then focuses on the application of nanoparticle and CNT properties to the enhancement of packaging materials for reliability, e.g. by melting-point depression, sintering, Coulomb blocks, enhanced chemical activities, high mechanical strength, low ballistic resistance, etc. At the same time it will discuss applications of nanowires and other nanoscale structures.

Course Outline:

(1) Introduction to Electronics Packaging and current trends: IoT, flex circuits, wearables, 3D thermal, embedded passives, etc.
(2) Introduction to Nanotechnologies in Electronics Packaging
(3) Nanoparticle properties: melting point depression, coulomb block, sintering, optical, etc
(4) Nanoparticle fabrication
(5) Nanoparticles for high-k dielectric capacitors and resistors for embedded passives
(6) Nanogranular magnetic core inductors for embedded passives
(7) Nanoparticles in electrically conductive adhesives,
(8) Nanoparticles in microvias and conductive inks for SMT interconnect
(9) Nanoparticles added to lead-free solders and flip-chip underfills
(10) CNTs: fabrication, characterization (chirality, etc), and properties
(11) CNT effects in solders
(12) CNTs for thermal management and electromagnetic shielding
(13) Graphene for thermal management
(14) Nanowires and nanoscale spring interconnects
(15) Current commercial applications of nanopackaging
(16) Nanoscale modeling and simulation

(17) Summary

The course will be beneficial to electrical, mechanical, and materials engineers alike, or anyone with an interest in electronic device design, fabrication, assembly, or application. The level will be introductory, and accessible to students and graduates in any of these areas or the physical sciences.

Biography

Jim is a Professor Emeritus of Electrical & Computer Engineering at Portland State University, Oregon, and at the State University of New York at Binghamton. His B.Sc. and 1st Class Honors M.Sc. degrees in Physics are from the University of Auckland, New Zealand, and his Ph.D. in Electrical Engineering is from the University of Saskatchewan, Canada. He has served as Department Chair at both Binghamton and Portland, and was the founding Director of Binghamton's Institute for Research in Electronics Packaging. Jim has also held faculty positions at Saskatchewan, Victoria University of Wellington (NZ), and South Dakota School of Mines & Technology, with visiting/sabbatical positions at Loughborough University (UK) as a Royal Academy of Engineering Distinguished Visiting Fellow, Chemnitz University of Technology (Germany), University of Maryland (USA), University of Bordeaux (France), University of Greenwich (London), Chalmers University of Technology (Sweden), Dresden University of Technology, University of Canterbury (NZ) as an Erskine Fellow, and Helsinki University of Technology as a Nokia-Fulbright Fellow, with honorary appointments at Shanghai University and Shanghai Jiao Tong University. Other positions have included Senior Technician and Post-Doctoral Fellow at the U of S, brief periods with Delphi Engineering (NZ) and IBM-Endicott (New York), and industrial consulting. He was recognized in 2015 with an honorary doctorate from the POLITEHNICA University of Bucharest.

Jim is an IEEE Fellow and an IEEE Components, Packaging, & Manufacturing (CPMT) Society Distinguished Lecturer. He has served as CPMT Treasurer (1991-1997) and Vice-President for Conferences (1998-2003), and currently sits on the CPMT Board of Governors (1996-1998, 2011-2016) and on the joint Oregon CAS/CPMT Chapter executive committee, and chairs the CPMT Nanotechnology technical committee. He was awarded the IEEE Millennium Medal and won the CPMT David Feldman Outstanding Contribution Award in 2005. He is an Associate-Editor of the IEEE CPMT Transactions and has been General Chair of three CPMT-sponsored conferences, Treasurer or Technical Chair of others, and serves on several CPMT conference committees. As the CPMT Society representative on the IEEE Nanotechnology Council (NTC), he instituted a regular Nanopackaging series of articles in the IEEE Nanotechnology Magazine, established the NTC Nanopackaging technical committee, (which also acts as a program committee for annual IEEE NANO conferences,) served as the 2010-2012 NTC Awards Chair, chaired the IEEE NANO 2011 conference in Portland, and served as NTC Vice-President for Conferences (2013-2014) and currently as Vice-President for Finance. He also co-founded the Oregon Chapter of the IEEE Education Society in 2005 and sits on its executive committee, and was Program Chair for the 1st and 2nd IEEE Conferences on Technology for Sustainability (2013/14).

His research activities are focused on electrically conductive adhesives, the electrical conduction mechanisms in discontinuous nanoparticle thin metal films, with applications to nanopackaging and single-electron transistor nanoelectronics, and on an NSF-funded project in undergraduate nanotechnology education. He has edited or co-authored five books on electronics packaging and two on nanodevices, and lectures internationally on nanopackaging and electrically conductive adhesives. He is currently putting together the expanded second edition of his book: "Nanopackaging: Nanotechnologies and Electronics packaging" (Springer, 2016.).

Professional Development Course 5

30nd November 2016 – 13:10 to 17:00hrs.

Internet of Things (IoT) focusing on Wireless Sensors Network and Active RFID

Holden Li

Tamasek Laboratory at Nanyang Technological University

Course Outline

This short course focuses on the technology and markets enabling the Internet of Things (IoT), especially related technologies such as Wireless Sensor Network and Active RFID. The class will discuss in detail generic IoT sensors, especially MEMS based one, that are commonly used and also upcoming ones; technologies progression over the past ten years and looking beyond; reality versus the hype, etc.

It will also specifically address issues like the hardware advantages and disadvantages for each choice. Participants will have a better understanding of what IoT is and which part does wireless sensing and RFID play. Other interesting topics include the architecture of IoT from the ground up; traditional Active RFID, RFID enabled cellphones, smart active labels/ battery assisted passive tags, and Wireless/Ubiquitous Sensor Networks (USN). Lastly, a brief introduction on the various energy harvesting mechanisms will also be discussed.

Course outline:

(1) Introduction and background of IoT
(2) RFID System Basics
(3) Various RFID related technologies used in IoT
(4) RFID related application in Singapore
(5) Wireless Sensor Networks (WSN)
(6) WSN in Singapore context
(7) Enablers of IoT – Energy Harvesting
(8) Real Time Location Systems
(9) Tradeoff studies of various technologies
(10) Related Opportunities in Singapore and South East Asia

Biography

Dr Holden Li graduated in NUS with a Bachelor of Engineering (Honors) in 1997. In 2000 Holden enrolled in Stanford University for his graduate studies under Professor Thomas Kenny. During his PhD studies, Dr Holden Li was actively involved in MEMS process development in finding suitable packaging solutions to MEMS and BioMEMS devices. Besides, he worked closely with several industrial partners who benefited from the on-going research

activities in Kenny's group at that time. He was awarded his MSc and PhD in Mechanical Engineering in 2001 and 2005 respectively. Back in Singapore in September 2005, he started to lead a research team in MEMS sensors research effort in the area of MEMS R&D and reliability study. Beyond this, his passion for R & D in microelectronics, and his strong academic interest in the area of micro and nanotechnology propelled him to seek for funding opportunity in this area. He is currently working closely with several senior faculties in the area of microelectronics, MEMS research and Internet of Things (IoT) applications both in NTU and Temasek Laboratories at NTU. He is serving on the National Committee of Semiconductor Devices

KEYNOTE

How to Feed Enough to Greedy IoT Monster

Kanji Otsuka

Meisei University, Japan

IoT changes greedy monster now-a-day. That seems to be uncontrollable world. Mega-data centers (DC's) are trying to catch the monster mainly in the US. These systems included even edge center ones are in blind as like fog weather because the DC's providers have been developed by own inside technologies. In our historically seen, the concept has been undergoing as "high-end technologies automatically shift to low-end ones". So we want to know what the blind out. In my experiences, some of specific examples show by that could reveal the blinds and get the evidence.

The most important element on their thought is communication bandwidth that is directly affected the data processing performance and communicating each other. The way for getting wider bandwidth involves three approaches which are high speed clocking, many lanes and high data compression. The first two issues relate with packaging technology which would be presented some. We additionally consider data compression technology. The system performance balance should put together the three issues. Let's focus in the three issues now.

While power saving is another one of the most important things in not only DC's but mobiles. Higher bandwidth introduces saving power that we should know. Architecture of data processing with low power is managed by packaging issues which focus in also.

If you well done of it, the world's highest-volume IoT platforms, the largest commercial health data clouds, the largest commercial video platforms and so on even in mobile fields could be taken as far as technological basis.

Biography: Kanji OTSUKA

Graduated from Kyoto Institute of Technology in 1958, with doctor's degree of material science from Tokyo Institute of Technology. IEEE Fellow in 1998.

Job functions:

Hitachi Ltd., from 1959, since thirty-four years, in semiconductor group firstly. That was dawn period for semiconductor technology, so learned from solid-state physics to basic production process with original technology development. And also charged in computer technologies belong main-frame group late of the period especially in high speed IO interface circuit and CPU-memory interconnection. Then large system design technology got for his knowledge. In such job experiences, having wide technologies in materials, wafer processing, packaging, circuit technologies and system design for the semiconductors and computers.

Since 1992, Meisei University, Faculty of Informatics, Dept. of Electronics and Computer Science as a professor. Also the Director of Graduate of Informatics from 1999 to 2000, and Dean of Faculty of Informatics from 2001 to 2003.

Current position; executive researcher and emeritus professor of Meisei University from 2006, Invited Professor of Osaka University (2011-now) and Guest Instructor of the University of Tokyo (2011).

His recent job; in the large system so-called concurrent total system design with high speed processing logic, memory LSIs and including wafer processing, packaging and materials.

INVITED PRESENTATION

Innovations in Packaging will enable the IoT world of the Future

Dr. W. R. Bottoms

Third Millennium Test Solutions

Technical Session: 1st December 2016, 13:30hrs

Venue : MR336

Moore's Law scaling can no longer maintain the pace of progress just when we need it most. Data, logic and applications are migrating to the cloud, consumerization of data and the rise of the Internet of Things are placing new demands and they are all occurring at the same time. Difficult challenges in power, performance, latency, bandwidth density and cost threaten our ability to maintain the progress that has enabled the growth of our industry. Meeting these challenges will require reduction in power and cost per function by a factor of 10^4 over the next 15 years while improving performance and decreasing latency. It is clear that we will not have a replacement for the CMOS switch in the near term to return to a device scaling path to maintain the pace of progress. Only a revolution in packaging, which has not kept up with the scaling of CMOS, can provide a solution. This will require new tools for design and simulation, new packaging architectures, production processes, materials, and equipment. These difficult challenges and potential solutions will be discussed.

BIOGRAPHY: WILMER R. BOTTOMS

Dr. Bottoms received a B.S. degree in Physics from Huntington College in Montgomery, Alabama in 1965, and a Ph.D in Solid State from Tulane University in New Orleans in 1969 and is currently Chairman of Third Millennium Test Solutions. He has worked as a faculty member in the department of electrical engineering at Princeton University, manager of Research and Development at Varian Associates, founding President of the Semiconductor Equipment Group of Varian Associates and general Partner of Patricof & Co. Ventures. He has served as Chairman and CEO of Several Companies both public and private.

Dr. Bottoms has also served in a number of Government Advisory positions including Chairman of the Board on Assessment for NIST and a member of the Technical Advisory Committee on export controls for the US Commerce Department.

Dr. Bottoms currently serves as:

- Emeritus Member of the Board of Tulane University
- Co-Chair of the Heterogeneous Integration Roadmap

- Chairman of the SEMI's Awards Committee
- Chairman of the Packaging and Package Substrates Technical Working Group for INEMI
- Member of the Board of MIT's Microphotonic Center
- Chairman of APMT
- Chairman of Third Millennium Test Solutions

INVITED PRESENTATION

In the IoT development frame: how to address mechanical and thermal issues?

S. Gallois-Garreignot

STMicroelectronics

Technical Session: 2nd December 2016, 8:30hrs

Venue : MR 331

Previous years have seen tremendous surge of interest and publications in the Internet of Things (IoT). Generally speaking, IoT may be defined as a global infrastructure connecting virtual and physical generic objects, collecting & exploiting information provided by those objects, and its related network developments. Numerous visions co-exist in the industry for that domain. The very wide range of possible applications (Transportation, Healthcare, Home/Office/Plant environments…) clearly promotes this technology as a real business opportunity in the coming years. In that regard, STMicroelectronics has developed a unique portfolio covering all the necessary building blocks (Analog, Connectivity, Microcontrollers, Power, Sensors…) able to provide solutions to create smart things.

In our analysis, IoT technologies rely on a strong heterogeneous integration, connectivity standards, large bandwidths and low power consumption… Moreover, the fields of application are as numerous as they are challenging. Indeed, the environments may be harsh and quite different from one to another: Automotive, Industry… Reliability may be also crucial like in e-Health domain. In that context, co-design is needed to propose reliable, optimized and efficient object. Focusing on the mechanical and thermal issues, these aspects have to be evaluated and controlled as soon as possible during the product development.

To do so, a traditional approach, based on Finite Element method, is necessary. Such tool may be considered as a good compromise between standardization/availability on the market, user-friendly interface and accuracy. However, the scale of interest (from millimeter to microns, and even nanometer) is a huge challenge which requires additional approaches.

Experimental characterization (properties, imaging, strain/temperature map…) is complex in our industry due to strong constraints: thin film effect, sample processing and micrometer scale are part of it. However, we have at our disposal very well-known electronic devices which can be rethought as sensors (among others, diode, transistor, resistance). Thus, it provides *in-situ* measurements during the process flow and/or the product life. Such data are more than welcome for our community: for calibration (CAD tool) and qualification (product) purposes but also, as an

important data bank which may be used for further optimization, knowledge of the stress state in various applications…

In that sense, the parallel with the IoT (interactions and communications with the environment thanks to sensors embedded in everyday-life objects) is interesting and may be inspiring for developing new approach/methods for the reliability.

Biography: Sebastien Gallois-Garreignot

Sebastien Gallois-Garreignot is in charge of mechanical and thermal simulations for STMicroelectronics, more particularly concerning the Chip/Package interactions and the related failures. Development of mechanical characterization methods, understanding of the fracture phenomena in complex architecture are ones of his additional fields of research and expertise.

He received Phd degree from INSA-Lyon on the experimental and numerical investigations on the fracture phenomena in advanced architecture in microelectronics in 2010.