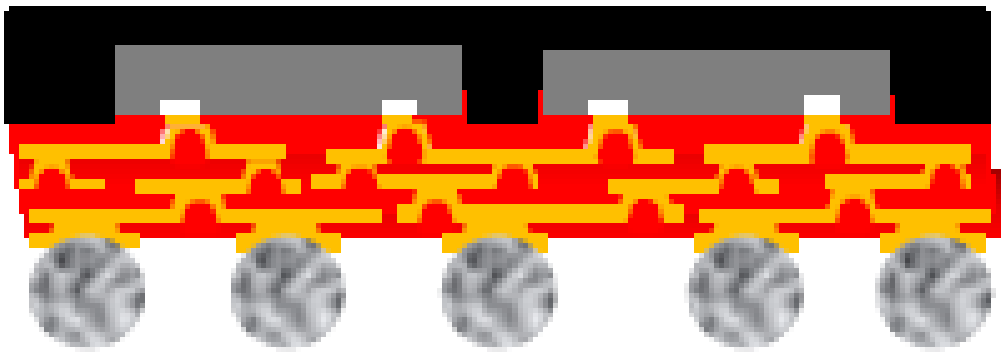
Fan-In Fan-Out Wafer Level Packaging



The mobile market is accelerating demand for more compact and complex semiconductor packages that are challenging traditional packaging technology in the areas of form factor, reliability and performance. This demand is driving the quick growth of conventional Fan-In wafer level packages (WLP), with estimated CAGR of 9% from 2014 to 2019. In another respect, the demand for high density interconnection, superior electrical performance and the ability to integrate multiple heterogeneous is driving the growth of new Fan-Out WLP, which is projected at CAGR of 87% from 2015 to 2020(from Techsearch)!

EPTC 2016 has lined up short courses on Fan-In Fan-Out WLP Packaging and 2 invited speakers to present on the advanced Fan-Out WLP. Full details are in the subsequent pages.

PROFESSIONAL DEVELOPMENT COURSES

Professional Development Course 3

30nd November 2016 – 13:10 to 17:00hrs.

Fan-In and Fan-Out in Wafer Level Packaging

Albert Lan

Senior Director, Engineering Center, SPIL, Taiwan

Course description:

The Wafer Level Package (WLP) continues to see strong growth driven by mobile phones, tablets, portable players, wearable and IoT devices with its benefits of small form factor and low profile packages.

In this course, we will introduce the innovative solutions of WLP include mold type WLCSP (mWLCSP), Fan-out Wafer Level Package (FOWLP). Also, the future trend will be covered Panel Level FO technology.

Course Outline:

1. Introduction
2. What is Wafer Level Package
3. Market Trend of Wafer Level Package
4. Innovative Package Solutions Introduction and Challenge
5. Molded WLP (mWLCSP)
6. Fan-Out WLP (FOWLP)
7. Future Package Solutions Introduction and Challenge
8. Panel Level Fan-Out (PLFO)
9. Summary

About the speaker:

Education:

Master of industrial & mechanical engineering department, Univ. of Wisconsin, Madison

Job Experience:

Over 20 years of job experience on semiconductor industry, especially focus on bumping and flip chip advanced assembly technology.

Vice Chairman of Semiconductor Equipment and Materials International Taiwan Association.

Chairman of TILA (Taiwan Intelligent Leader Association)

Now :

Senior Director of Engineering Center of SPIL (Siliconware, Taiwan), which is 3rd biggest assembly house in the world now

INVITED PRESENTATION

Multi-die integration using advanced fan-out packaging technology

WonChul Do

AMKOR

Technical Session: 2nd December 2016, 13:40hrs

Venue : MR332

The ability to integrate multiple die, passives components, and even packages is one of the key enablers for the widespread adoption of Fan-Out Wafer Level Package (FO-WLP). The other restrictions or challenges of traditional FO-WLP are limited line and space capabilities, creation of 3D structures, and good die scrapping concerns associated with chip first flow. Chip last and RDL first fan-out approach can overcome many of the issues associated with conventional fan-out technology and provide increased I/O and circuit density within a reduced footprint and profile. This presentation describes the process flow of a new chip last high density fan-out technology and compares its package capabilities with flip chip based 3D PoP at 15 mm package size. The results show the new chip last FO-WLP has better electrical and thermal performance with very robust component and board level reliability. More complicated SiP and its further miniaturization can be realized because RDL formation is done without any mold compound before chip attach is performed and the creation of advanced 3D structures and integration of passives with various surface finishes are possible. For the most aggressive designs such as interconnect for split die architecture or for High Bandwidth Memory (HBM), 2.5D interposer with fine line damascene Cu BEOL must be incorporated. For high performance and multi-die mobile products, FO-WLP with TSV-less interposer and chip last process flow can provide the 2.5D sub-micron routing capability, lowers cost, and improves electrical performances. The routing capability, process flow, and reliability results of a TSV-less package TV with 15 mm body will be presented.

Biography

WonChul Do is Sr. director of R&D Division Group and currently leading the development of next generation fan-out packaging technology at Amkor Technology Korea, Inc. He was package development project manager for 2.5D/TSV products until he took on the current role in 2014. He has more than 15 year experience in the semiconductor packaging field and has been involved in the development of flip chip package, wafer bumping and wafer level packaging and 2.5D/3D IC packaging. He received a Master of Science degree in Electronic Engineering from Sogang University in Seoul, Korea.

Materials and Processes of Fan-out Wafer/Panel Level Packaging

Li Ming

ASM

Technical Session: 2nd December 2016, 13:40hrs

Venue : MR333

The presentation will focus on the design, materials, process, and equipment of fan-out wafer/panel-level packaging (FOWLP or FOPLP). Various FOWLP formation methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first) will be introduced. Several key process technologies, such as die pick & place, molding, redistribution layer (RDL) and solder ball mount will be discussed. Since warpage control is a critical issue for the process, effects of various factors, such as molding material property, chip size, EMC thickness and package fan-out ratio, on the wafer/panel warpage will be studied. Based on the applications, different RDL process (Cu damascene, polymer thin film, or printed circuit board (PCB) approach), RDL line/width, dielectric thickness, and equipment involved will be recommended and summarized.

Biography

Li Ming was awarded BSc and MSc in Materials Science and Engineering by Shanghai Jiao Tong University, China, and earned her PhD in Materials Science from the University of London, UK. Before joining ASM in June 2004, Dr. Li Ming worked in the University of London (UK), the Institute of Materials Research and Engineering (Singapore), and Chinese University of Hong Kong (Hong Kong). Currently, working in ASM as a R&D Director for Enabling Technology, Dr. Li is heading the Process and Packaging Technology Development Team to improve current processes and explore advanced packaging technologies. Dr. Li has published more than 70 papers in leading journals & technical conferences.